WHAT IS CLAIMED IS:

1. A write compensation circuit of a recording device comprising:

a first delay portion driven by a first driving voltage, for receiving a clock signal, delaying the clock signal by a first delay time, and outputting the delayed clock signal; and

a voltage supplying portion for supplying the first driving voltage to the first delay portion in such a manner that the first delay time is substantially equal to a clock period of the clock signal.

2. A write compensation circuit according to claim 1, wherein:

the voltage supplying portion comprises:

a second delay portion driven by a second driving voltage and having the same configuration as that of the first delay portion, for receiving a clock signal, delaying the clock signal by a second delay time, and outputting the delayed clock signal;

a determining portion for determining whether the second delay time is within a predetermined range; and

a voltage select portion for selecting, according to a result of determination of the determining portion, the first driving voltage supplied to the first delay portion and selecting the second driving voltage supplied to the second delay portion.

3. A write compensation circuit according to claim 2, wherein:

the first delay portion comprises:

a selector for selecting a predetermined pattern in

response to a select signal; and

a delay circuit for delaying the clock signal by a delay amount corresponding to the predetermined pattern selected by the selector.

4. A signal interpolation circuit wherein a pair of input signals having different phases are split into a pair of output signals having a phase similar to that of the pair of input signals, respectively, and an output signal having a phase intermediate between the phases of the pair of output signals; and by comprising a plurality of elements, the pair of output signals and the output signal having the intermediate phase have substantially the same propagation speed,

the signal interpolation circuit further comprising:

a control section for controlling the propagation speed.

5. A signal interpolation circuit according to claim 4, wherein the control section controls propagation speeds of input and output signals into and from each of the plurality of elements.

6. A signal interpolation circuit according to claim 4, wherein the control section controls speeds of input and output signals into and from each of the plurality of elements.

7. A signal interpolation circuit according to claim 4, wherein the control section adjusts propagation speeds of input and output signals into and from each of the plurality of elements in accordance with the phase difference of the pair of input signals.

8. A signal interpolation circuit according to claim 4, wherein the control section adjusts propagation speeds of input and output signals into and from each of the plurality of elements in accordance with a change in the phase difference of the pair of input signals.